Special session: Hot topics: Statistical test methods

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Special Session: Hot Topics: Statistical Test Methods

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The process of testing Integrated Circuits involves a huge amount of data: electrical circuit measurements, information from wafer process monitors, spatial location of the dies, wafer lot numbers, etc. In addition, the relationships between faults, process variations and circuit performance are likely to be very complex and non-linear. Test (and its extension to diagnosis) should be considered as a challenging highly dimensional multivariate problem.

Advanced statistical data processing offers a powerful set of tools, borrowed from the fields of data mining, machine learning or artificial intelligence, to get the most out of this data. Indeed, these mathematical tools have opened a number of novel and interesting research lines within the field of IC testing.

In this special session, prominent researchers in this field will share their views on this topic and present some of their last findings. The first talk will discuss the interest of likelihood prevalence in random fault simulation. The second talk will show how statistical data analysis can help diagnosing test efficiency. The third talk will deal with the reliability of Alternate Test of AMS-RF circuits. The fourth and last talk will address the idea of mining the test data for improving design manufacturing and even test itself.

A. ***Random sampling for fault simulation: intuition vs. theory and reality****, by Stephen Sunter*

Most engineers understand the theory of random sampling, but often their intuition is inconsistent with the theory or reality. Theory for a new likelihood-weighted random sampling technique was presented in our ITC 2014 paper [1]. This presentation provides real examples of inconsistencies based on experiences with a commercial analog fault simulator at multiple companies. The examples: intuition says that simulating more defects might produce a higher estimated coverage, but theory shows this is unlikely; intuition says that pre-simulation analysis of a circuit could reveal defects that do not need to be simulated, but reality shows this is impractical; intuition says you need to simulate at least a few percent of all potential defects, but theory shows otherwise; intuition says that coverage of portions of a circuit can be gleaned from results for faults randomly injected into the whole circuit, but theory shows otherwise; intuition says you must simulate coverage of every defect type, but reality shows otherwise; intuition says that improving a test to detect the most-likely defects that were undetected will have the greatest impact on coverage, but theory shows otherwise. We conclude that likelihood-weighted random sampling is more general and practical than other approaches for reducing fault simulation time, but its efficiency can be counter-intuitive.

B. ***Targeting Opens versus TDF in Two-Pattern Scan Testing: What Defect Statistics May Be Telling Us****, by Adit D. Singh*

Industry has now had over a decades worth of experience with scan based TDF timing tests, yet many questions still remain regarding the effectiveness of this methodology, and even how it is best applied. Many companies strongly believe that launch-on-capture (LOC) tests alone are sufficient for screening manufacturing defects since they can test all transitions between functional states that are encountered in normal functional operation; this view also often holds that launch-on-shift (LOS) tests can potentially lead to 'overtesting' and yield loss. Others consider LOS timing tests essential for high TDF coverage and are willing to make the design-for-test (DFT) investment in timing closed scan enable control signals needed to support at-speed LOS testing. So what physical defects are we really catching with each type of test? Are we 'overtesting'? Is small delay testing worth the extra test cost and potential yield loss? These questions can only be reliably answered with detailed statistics from volume production tests on a range of manufactured parts.

In the absence of such comprehensive data, at least in the public domain, we piece together the best available evidence and show that it appears to challenge conventional wisdom and current test practice. We make the case that TDF tests, even when applied with aggressive timing, appear to mostly detect open defects, the majority of which can be detected at somewhat slower test speeds without the risk of unnecessary yield loss from test noise. Meanwhile, many other open defects that can cause operational failures remain undetected by current LOC, and even LOS, TDF tests, as has been shown by recently published studies with Cell-Aware tests. These test

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escapes can significantly compromise product defect levels. However, even Cell-Aware tests currently do not target a significant class of open defects that appear to be redundant but can in fact frequently cause functional failure due to circuit hazards. We therefore suggest that it may be better for two-pattern tests to explicitly target all open faults in the circuit, with the tests being applied at the highest possible speed that avoids yield loss from test noise. TDF faults will implicitly be covered by such an approach.

C. ***Statistical techniques and metrics for alternate testing of analog/RF integrated circuits****, by Florence Azaïs*

The concept of alternate testing emerged in the late 90s with the objective to reduce testing costs of analog integrated circuits by replacing the conventional specification measurements with a single transient acquisition using a carefully optimized test stimulus [2], [3]. This concept has then been extended to RF circuit testing with the objective to replace the costly RF performance measurements by simple low-cost indirect measurements. In both cases, the fundamental idea of the technique is to exploit the underlying relationships that exist between indirect measurements and conventional measurements in order to build prediction models that permit to evaluate the device performances using only the low-cost indirect measurements. Because these relationships are non-trivial, statistical methods have to be used to build prediction models.

This approach has been widely explored and demonstrated in the literature on various case studies over the past twenty years. However alternate testing is still not widely used in industry mainly because of a lack of confidence in the achieved test efficiency. Many factors influence this efficiency such as the choice of adequate indirect parameters, the choice of the prediction model, the order of mapping between indirect measurements and device specifications, or the size and composition of the training set. The objective of this talk is to discuss various statistical methods for the choice of adequate indirect measurements [4]–[7], pertaining to both filter and wrapper categories in the field of feature selection. Their impact on alternate test efficiency will be evaluated in terms of model and prediction accuracy by using classical metrics such as average and maximal errors, but also in term of prediction reliability by introducing a new metric called Failing Prediction Rate (FPR). Results are illustrated on two case studies for which we have experimental test data, i.e. a power amplifier and a RF transceiver.

D. ***What Gold can be Mined from Test Data?****, by Shawn Blanton*

Test data can take on many forms, ranging from pass-fail information for both binary and analog tests, to various parametric measurements that include min VDD and IDDQ to full-blown quantification of various specifications. Undoubtedly these measurements are taken to determine if the circuit under test is functioning as desired. It is becoming more and more evident however that there is valuable information, beyond go/no-go, that is hidden within the test data. The challenge however is developing sound methodologies that deconvolute the test data in order to make statistically-significant conclusions about the information derived.

For over ten years now, researchers in the Advanced Chip Testing Laboratory (www.ece.cmu.edu/ actl) have and continue to develop various methodologies for mining test data to uncover actionable information for improving design, manufacturing and even test itself. A key enabling technology is software-based diagnosis, a topic of significant interest as of late because of its role in test-data mining. In this talk, we will make a case for all the gold that can be mined from test data and the challenges involved that range from having a precise and accurate chip-level diagnosis methodology to obtaining significant levels of data for making sound conclusions using actual in-production chips. Finally, we will make the case for increasing the fidelity of test-data mining through the design and fabrication of product-like test chips which are actual ICs that are designed to be highly testable and diagnosable while at the same time reflecting characteristics of actual customer designs.

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